COLLEGE OF ENGINEERING
Electrical & Computer Engineering

ECE 274A: Digital Logic

Spring 2025

Instructor:	Dr. Jyotikrishna Dass	**Lecture Time:**	MWF 10:00 – 10:50 AM
Email:	jdass@arizona.edu	**Lecture Venue:**	Education, Rm 353

"Nothing is more important than seeing the sources of invention which are, in my opinion, more interesting than the inventions themselves." Leibnitz (1646-1716)

Contents

Course Pages

1. D2L → for general announcements and course materials.
2. Microsoft Teams → for discussions on lectures, labs, quizzes, and assessments.

Teaching Crew

- **Instructor:** Dr. Jyotikrishna Dass | Office: ECE 456T | Office Hours: See D2L or by appointment
- **Teaching Assistants:** Zhuangzhuang Chen and Chieh Tsai | Office Hours: See D2L

Course Prerequisites

ECE 175 or ECE 101. Prerequisite or concurrent enrollment in MATH 129.

Course Format

- **Lecture:** in-person | MWF 10:00 – 10:50 AM | Education, Rm. 353
- **Lab:** in-person | Students will attend the registered lab session (001A/C/E) | ECE, Rm 301 | Mo/Tu 2:00 – 4:50 PM and Th 11:00 – 1:50 PM

Equipments and Software Requirements

For this course, you will need a computer or laptop (preferably with Windows). For lab activities, we will use two separate software tools to complete and test various hardware chips. For download instructions, please refer to D2L.

- `nand2tetris online IDE:` This is a web-based interactive hardware simulator for chips written in a pedagogical Hardware Description Language (HDL).
- `AMD/Xilinx Vivado Design Suite:` This software suite is used for the synthesis and analysis of industry-leading Verilog HDL designs, which will be implemented on FPGA devices in the lab.

Textbook (required)

- If you use Pay One Price, see D2L for accessing zyBooks.
- If you do not use Pay One Price, buy the book using the steps below.
  - Sign up or create an account at zyBooks. Use U of A email address (.arizona.edu).
  - Enter zyBooks code: `ARIZONAECE274ADassSpring2025`
  - Choose Section 1, click 'Subscribe'. A subscription is $64. Subscriptions will last until May 30, 2025.

References

This is a list of interesting and useful books that you could consult occasionally. It is highly likely that online or physical copies may be available at University of Arizona Libraries. Purchase is **not** required.

- Frank Vahid, *Digital Design with RTL Design, VHDL, and Verilog*, John Wiley & Sons Inc; 2nd edition (January 1, 2010). zyBooks was created by Frank Vahid to digitize this very book. We are using the zyBooks version as required textbook.
- Noam Nisan, and Shimon Schocken, *The Elements of Computing Systems: Building a Modern Computer from First Principles*, The MIT Press, 2nd edition (June 15, 2021). nand2tetris book - The first half of the textbook is available free online.
- David A. Patterson, and John L. Hennessy, *Computer Organization and Design MIPS Edition: The Hardware/Software Interface*, Morgan Kaufmann; 6th edition (December 4, 2020).

  Alternatively, David A. Patterson, and John L. Hennessy, *Computer Organization and Design RISC-V Edition: The Hardware Software Interface*, Morgan Kaufmann; 2nd edition (December 31, 2020).

Important Dates

- **1/15/25:** First day of classes
- **1/20/25:** No classes - Martin Luther King Jr. Day
- **1/22/25:** Last day for students to use UAccess to add classes and swap classes or class sections
- **1/28/25:** Last day to drop a course **without** a grade of W on your transcript
- **3/8/25–3/16/25:** No classes - Spring recess
- **4/1/25:** Last day to drop a course, **with** a grade of W, through UAccess. After this time, signature of the instructor and an approval of the students' college Dean is required
- **5/7/25:** Last day of classes and laboratory sessions
- **5/8/25:** No classes or finals - Reading day

Access complete list at https://registrar.arizona.edu/dates-and-deadlines and https://catalog.arizona.edu/academic-calendar#2024-20251. For course scheduled dates, refer to Page 8.

Course Objectives

Welcome to the fascinating world of digital logic! In this course, we will embark on an exciting journey to uncover the secrets of how computers work and how they are designed. Together, we'll dive into the basics of how we represent numbers in computers and the essential ideas behind creating digital circuits. We'll start with number systems, which are the different ways we can represent numbers in a computer, like binary (using only 0s and 1s). Understanding this is crucial because computers use these systems to process and store data.

Next, we'll explore fundamental digital design concepts. This includes:

- **Combinational circuit design:** These are circuits where the output depends only on the current inputs. Think of it like a simple calculator that gives you an immediate result based on the numbers you input. In a computer, combinational circuits are used in components like the Arithmetic Logic Unit (ALU), which performs arithmetic and logical operations. The ALU takes input data and performs operations like addition or comparison, providing an immediate output.
- **Sequential circuit design:** These circuits have memory, so their output depends on the current inputs and the history of past inputs. A great example is a traffic light controller. It changes lights in a sequence based on a timer and the current state (e.g., green to yellow to red), and it needs to remember the current state to know what comes next. In a computer, sequential circuits are used in components like memory registers and counters. For instance, the Control Unit in a CPU uses sequential logic to manage the execution of instructions, keeping track of the current instruction and what comes next.
- **Register-transfer level (RTL) design:** This is a way of designing circuits at a higher level, focusing on how data moves between registers (storage elements) and how the data is processed. In a computer, RTL design is used to describe the operations of the CPU and other complex digital systems. It involves specifying how data is transferred between registers and how it is manipulated by the ALU and other components. RTL design helps in planning and optimizing the flow of data within the computer, ensuring efficient processing and performance.

Imagine building a general-purpose computer system from the ground up—sounds thrilling, right? That's exactly what we'll do! You'll get hands-on experience through captivating lab projects where you'll design and implement digital components. These components will come together to form complete digital systems, giving you a real sense of accomplishment. You will also get to write Hardware Description Language (HDL) to describe your digital creations and bring them to life using a development FPGA board. This course is not just about learning; it's about creating, exploring, and having fun with digital logic.

Why learn about Digital Logic?

Digital logic is the gateway to understanding the incredible world of technology that powers our daily lives. Imagine being able to peek under the hood of your favorite gadgets and truly grasp how they work. From smartphones and computers to smart home devices and cutting-edge robotics, digital logic is at the heart of it all. By diving into digital logic, you'll unlock the secrets of how digital systems operate. You'll learn about binary numbers, the language of computers, and how simple logic gates can be combined to create complex circuits. This knowledge is not just theoretical; you'll get hands-on experience designing and building real-world digital logic components. Imagine the thrill of seeing your own digital creations come to life!

This course will also set the stage for advanced topics like computer architecture, embedded systems, and VLSI design. Mastering digital logic will give you a solid foundation to excel in these areas, opening doors to exciting career opportunities. Companies like Intel, NVIDIA, and Qualcomm are always on the lookout for talented individuals with strong digital logic skills. Moreover, digital logic is relevant across multiple engineering disciplines. Whether you're interested in robotics, telecommunications, software development, or machine learning, understanding digital logic will help you design more efficient and effective systems and software programs. It's a critical skill that will make you a versatile and sought-after engineer.

So, get ready to embark on an exciting journey where you'll not only learn how things work but also create and innovate. Let's make this an unforgettable adventure in digital design!

☰ Course Topics

Here's a sneak peek at the fascinating topics we'll explore together.

- **Number systems and signed numbers:** Discover how computers represent and manipulate numbers, including binary and signed numbers.
- **Hardware Description Language:** Learn the language of digital design and how to describe complex circuits througe code and software tools.
- **Combinational Logic:** Dive into Boolean algebra and the design process for creating basic combinational components like logic gates.
- **Sequential Logic:** Explore the world of memory with basic storage elements and the design process for sequential circuits.
- **Datapath Components:** Get hands-on with designing adders, subtractors, multipliers, comparators, multiplexors, ALUs, multifunction registers, shifters, counters, timers, and register files.
- **Register-transfer level design:** Understand how data moves within a system and how to design efficient data paths.
- **Tradeoff or Optimization of digital circuits:** Learn how to balance performance, cost, and power consumption in your designs.
- **Physical Implementation and FPGA Overview:** See how your designs come to life on FPGA boards and understand the physical aspects of digital circuits.

Expected Learning Outcomes

By the end of this course, you will be able to

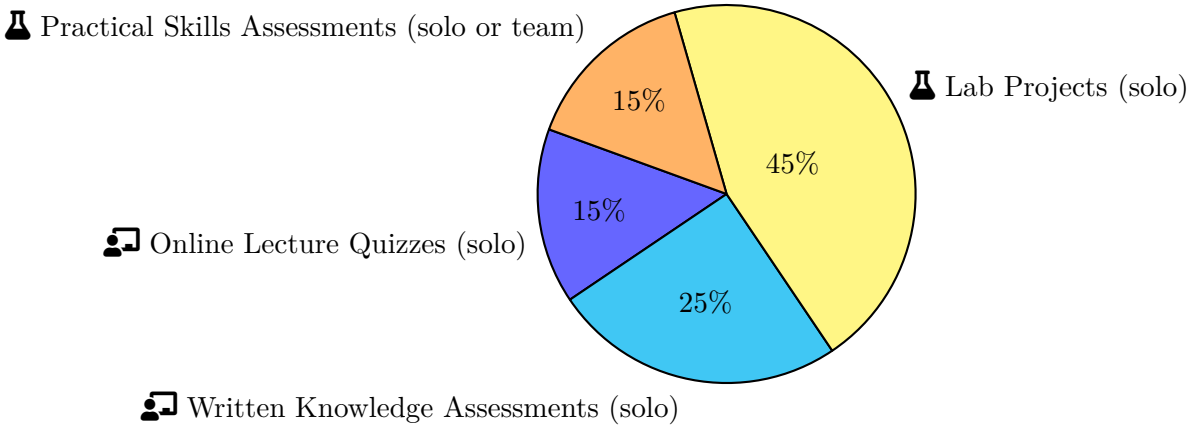
1. Represent any given integer number in different bases (such as base 2, 8, 10, and 16)
2. Explain the different binary representations of signed integers (sign magnitude, 1's complement, 2's complement) and use the 2's complement format to represent any given integer numbers.
3. Analyze combinational logic circuits using Boolean Algebra properties, Karnaugh map.
4. Design combinational logic circuits using combination logic design process
5. Analyze sequential logic circuits using appropriate tools
6. Design sequential logic circuits using sequential logic design process
7. Describe the structure and operation of Datapath components such as adder, comparator, ALU, multi-function register
8. Use the principles of register-transfer level (RTL) design and high-level state machines to analyze and design digital systems.
9. Design digital circuits using Hardware Description Language.
10. Use industry standard software design suite and programmable devices such as FPGAs to implement digital circuits.

Grading Scale and Policy

Letter Grade will be assigned based on the following grading scale. Requests for incompletes (I) and withdrawal (W) must be made in accordance with University policies which are available at *Grades & the Grading System | University of Arizona Catalog* and *Change of Schedule (Add/Drop) | University of Arizona Catalog*.

%Total	**≥90**	**80-89**	**70-79**	**60-69**	**<60**
Letter Grade	A	B	C	D	E

Grade Distribution: You will earn grade based on following lecture and lab activities.



(i) Lecture Activities

- **Online Lecture Quizzes (15%)** are aligned with weekly lecture content to build and apply fundamental concepts to problem solving (*remote, D2L, individual, open notes, two attempts with highest attempt as grade, no late submission, no make-up*).
- **2 Written Knowledge Assessments (10%+15%= 25%)** correspond to midterm and final exams (*class, individual, one letter-size page of reference guide that is self hand-written - no scanned/photocopy - allowed and needs to be submitted, no late submission, make up possible in certain cases; see Make-Up Policy on Page 7*).

(ii) Lab Activities

- **6 Lab Projects (45%)** are aligned with the course lecture content and help us reinforce the in-class learnings and vice-versa. During the lab, you will gain complete understanding of digital design from theory to practice, and learn industry-relevant skills in design, development, debugging and testing. *Make up possible in certain cases; see Make-Up Policy on Page 7.*

  Some portion of the lab projects may be assigned as hand-written lab worksheet for related theoretical work during lab hours (*lab, individual, open notes, submit to TAs*). You may need to work outside of the regular lab sessions to complete the "programming" portion of your lab projects. However, the written lab worksheet, FPGA implementation and demo to the TA, which constitute the major portion of your lab project grade, *must be done in-person during your assigned lab session.* Therefore, it is *highly recommended* to review the class materials and come prepared to make the most of the limited lab hours.

  (Collaboration Policy in Lab) While working in the lab on your lab projects, *two students* will be sharing the workbench with an FPGA device. Each team must comprise students from the same lab session. While you are encouraged to discuss the general principles and methods taught in the course and how they apply to the problem at hand, *sharing your specific solution is not permitted.* Please do not view or copy another student's solution, and do not allow another student to view or copy your solution. If you have any questions or need further clarification, feel free to ask. We're here to help you succeed! When submitting your lab project, you must acknowledge all resources not limited to slides, textbooks, TA, peer students, lab partner you may have referenced or consulted for the lab project.

  Each student in the team will need to submit their work individually on the D2L dropbox. You must demo your design to the TA during the lab hours before your D2L submission. Please be diligent with your lab projects as they are crucial milestones in preparing for the Practical Skills Assessments, where you will need to demonstrate your lab skills *individually*, unless specified otherwise.

  (Bonus Points) 5% will be awarded if the lab project is submitted by the "Incentive date". In addition, each lab project will also have "Last accepted date" which is the drop-dead submission deadline beyond which lab project submissions will *not* be accepted and *zero points* will be assigned for that lab project.

- **2 Practical Skills Assessments (7%+8%=15%)** First assessment is *in-lab (individual)* while the second assessment is *take-home with open notes (option of individual or a team of two). Make up possible in certain cases; see Make-Up Policy on Page 7.*

  (Practical Skills Assessment 1) For the in-lab skills assessment, each individual student will have **75 minutes** (first half or second half of assigned lab session) to design, test, demo, and submit their work for a given problem in the designated D2L Dropbox. You will have access to *one letter-size page as self-created reference guide (to be submitted to TA after assessment, TA may ask to see your notes).*

  (Not Allowed) calculator, email, smart phone, Internet (except D2L and zyBooks), and sharing of any resources or electronics with other students.

(Practical Skills Assessment 2) For the take-home skills assessment, you will have an *option to work by yourself or form a team of two students* to design, test, and submit your work for a given problem in the designated D2L Dropbox. Nonetheless, each student in team must submit the work individually on the D2L dropbox. **(Demo)** There will be a window of *one week* to demo your designs to the TA (if in team, both members must be present together for the demo) during any lab session in the demo week.

(Bonus Points) will be awarded as per following, if you score ≥50/100 in Practical Skills Assessment 2.

- **Individual:** Bonus is worth 10% of your original points. For instance, if you receive 65/100 by taking the second skills assessment all by yourself, your final points will be 65+(0.1×65)= 71.5/100. If you receive 45/100, your final points will stay at 45/100.
- **Team:** Bonus is worth 5% of your original points and both students will receive the same points. That means in above example scenarios, each member of the team will then receive 65+(0.05×65)= 68.25/100 (if original score was 65/100), and receive 45/100 (if original score was 45/100).

Make-up Policy: We understand that sometimes unexpected situations arise, and we offer the following scenarios where a make-up assessment or project is possible. However, please note that personal technology issues are not considered a valid excuse for missing a course requirement or deliverable. To avoid any problems, ensure your computer is properly configured and address any issues well in advance of submission deadlines. All dates and times mentioned in this course are in Mountain Standard Time (Arizona), which is UTC-7 hours. Arizona does not observe Daylight Saving Time.

- **Knowledge and Skills Assessments:** Make-up assessments, including both written knowledge and practical skills, are available only under extraordinary circumstances. If you need a make-up assessment, please reach out to me well in advance and provide written documentation explaining why you cannot attend the scheduled assessment. In cases of documented illness or personal emergency, kindly submit a written explanation via email along with supporting documentation **within three business days** of the missed assessment. Acceptance of the justification is at the instructor's discretion.
- **Lab Projects:** If you are unable to submit your lab project by the original deadline due to documented illness or personal emergency, you may request an extension. Please contact me well in advance (if possible) but **no later than three business days** from the original deadline. Provide supporting documentation via email explaining your situation. Acceptance of the justification is at the instructor's discretion.

(Late Submission Policy) Please note that late submissions are *not accepted* for Written Knowledge Assessments, Practical Skills Assessments, and Lab Projects. If these activities are not submitted by the deadline and there is no documented notification of a planned absence **before or within three business days** as described above for make-up, **zero points** will be assigned. For online lecture quizzes, there are no make-up opportunities, and late submissions will also receive **zero points**. The quizzes will automatically close at the deadline and the solutions will be provided. If you have any concerns or need further clarification, please feel free to reach out. We're here to support your learning journey!

(2 Late Project Waiver Tickets) We understand that academic life can be challenging, with students juggling multiple courses and commitments. To help manage these demands, we are offering **Late Project Waiver Tickets**. Each student is allowed **only two** "waiver tickets" for the lab projects (not the practical skills assessments). Each ticket can be used to submit a lab project *up to 24 hours late* from the "last accepted date" *without late penalty*. You can either apply both tickets to a single lab project for a total extension of 48 hours, or use them for two separate projects, granting a 24-hour extension for each. When you realize you may not be able to meet the upcoming deadline, notify the instructor as soon as possible to use your waiver ticket(s). Once the project deadline has passed and you have not notified the instructor earlier, you *cannot* use the late

waiver ticket for that project, and it will be assigned *zero points* according to our late submission policy. If you opted for this waiver ticket(s) and were still not able to meet the extention, **zero points** will be assigned and you would lose the ticket(s) for future projects. Therefore, we recommend to use this ticket judiciously and for reasons beyond personal emergency or documented illness (which fall under Make-Up Policy on Page 7). You must continue to adhere to code of academic integrity during this extention period.

Course Schedule

See the (tentative) Semester plan on D2L.

Practical Skills Assessment 1 (7%) ..... Mo/Tu/Th, Feb. 17/18/20 (Lab)
Written Knowledge Assessment 1 (10%) ..... We, Mar. 05 (Lecture)

Spring Recess ..... Mar. 8 - Mar. 16

Practical Skills Assessment 2 (8%) ..... Mo/Tu/Th, Apr. 28/29, May 01 (Lab)
Written Knowledge Assessment 2 (15%) ..... Fr, May 09 (10:30 am – 12:30 pm)

Code of Academic Integrity

- Students are encouraged to share intellectual views and discuss the principles and applications of course materials freely. However, graded work/exercises must be the product of independent effort unless otherwise instructed. Students are expected to adhere to the UA Code of Academic Integrity as described in the UA General Catalog. See *CODE OF ACADEMIC INTEGRITY | Dean of Students Office (arizona.edu)*.
- The University Libraries have some excellent tips for avoiding plagiarism available at `http://new.library.arizona.edu/research/citing/plagiarism`.
- In ECE 274A, this policy will be applied to all work submitted for a grade, including written knowledge assessments, practical skills assessments, online lecture quizzes, and lab projects. Copying previously posted solutions, solution manuals, and work of other students are s*trictly forbidden*; *All work must be original*.

  We will *not* be using generative AI tools such as ChatGPT, Copilot, and similar large language models in this 2xx level course to generate solutions because it is essential for you, as students, to develop a strong foundational understanding of the topics in this introductory Digital Design course and the ability to solve problems independently (unless mentioned otherwise). Relying on AI-generated solutions can hinder the learning process and prevent you from gaining the skills and knowledge necessary to succeed in higher-level courses and become a competent engineer.

  The minimum penalty for submitting work that is not your own is an E grade. The instructor is required to report violators of this policy to the Dean's office.

Accessibility and Accommodations

At the University of Arizona, we strive to make learning experiences as accessible as possible. If you anticipate or experience barriers based on disability or pregnancy, please contact the Disability Resource Center (520-621-3268, `https://drc.arizona.edu/`) to establish reasonable accommodations.

Los Angeles Wildfires Support

Many members of the U of A community come from or have ties to Southern California. Student Affairs has many resources to assist and support students impacted by the wildfires. If you're not ready to reach out just yet, or if you're still processing the information you've received and the situation as it unfolds, we understand and will be here for you whenever you feel ready to connect. Please don't hesitate to contact us when you need support. https://studentaffairs.arizona.edu/los-angeles-wildfires-support.

Safety on Campus and in the Classroom

For a list of emergency procedures for all types of incidents, please visit the website of the Critical Incident Response Team (CIRT): https://cirt.arizona.edu/case-emergency/overview.

Also watch the video available at https://arizona.sabacloud.com/Saba/Web_spf/NA7P1PRD161/app/me/ledetail/crtfy000000000003841.

Subject to Change Statement

Information contained in the course syllabus, other than the grade and absence policy, may be subject to change with advance notice, as deemed appropriate by the instructor.

Additional Syllabus Policies

Please refer to https://catalog.arizona.edu/syllabus-policies for various university policies and additional campus resources for students such as Campus Health, Counseling and Psych Services (CAPS), The Dean of Students Office's Student Assistance Program, Campus Pantry, and Survivor Advocacy Program.